WHAT IS CLAIMED IS:

1. A microcontroller comprising:

a central processing unit executing a program including an instruction that causes the central processing unit to activate a halt signal, to stop executing the program until an interrupt signal is received, then to inactivate the halt signal;

a memory storing data including said program, receiving a mode signal, outputting the stored data when the mode signal is inactive, and discontinuing output of the stored data when the mode signal is active; and

a control circuit receiving the halt signal from the central processing unit, wherein,

when the halt signal is activated, the control circuit reads a certain part of the program from the memory, internally stores said part of the program, then activates the mode signal; and

when the halt signal is inactivated, the control circuit inactivates the mode signal and supplies the central processing unit with the internally stored part of the program.

2. The microcontroller of claim 1, wherein the control circuit comprises a plurality of data latches for storing said part of the program.

3. The microcontroller of claim 1, wherein the control circuit comprises a first-in-first-out memory for storing said part of the program.

4. The microcontroller of claim 1, wherein the central processing unit generates a first address signal, and the control circuit comprises:

an address control unit generating a second address signal for reading said part of the program; and

a selector receiving the first address signal and the second address signal, selecting the first address signal when the halt signal is inactive, selecting the second address signal when the halt signal is active, and supplying the selected address signal to the memory.

5. A microcontroller comprising:

a central processing unit executing a program including an instruction that causes the central processing unit to activate a halt signal, to stop executing the program until an interrupt signal is received, then to inactivate the halt signal;

a memory storing data including said program, receiving a mode signal, outputting the stored data when the mode signal is inactive, and discontinuing output of the stored data when the mode signal is active; and

a control circuit through which the interrupt signal is passed to the central processing unit, wherein,

when the halt signal is activated, the control circuit activates the mode signal; and

when the control circuit receives the interrupt signal, the control circuit inactivates the mode signal, waits for the memory to resume data output, then sends the interrupt signal to the central processing unit.

6. The microcontroller of claim 5, wherein the control circuit comprises a counter for generating a delay from input of the interrupt signal to output of the interrupt signal.

7. The microcontroller of claim 6, wherein the control circuit comprises a logic gate for passing the interrupt

signal to the central processing unit, said logic gate receiving the interrupt signal and an output signal from the counter.

8. The microcontroller of claim 5, wherein the control circuit receives a signal from the memory indicating that the memory is ready to resume data output.

9. The microcontroller of claim 8, wherein the control circuit comprises:

a flip-flop delaying said signal from the memory;

an inverter inverting said signal from the memory; and

a logic gate for passing the interrupt signal to the central processing unit, said logic gate receiving the interrupt signal, the delayed signal from the flip-flop, and the inverted signal from the inverter.

10. The microcontroller of claim 5, wherein the control circuit comprises a flip-flop for generating the mode signal, said flip-flop being set by the halt signal and reset by the interrupt signal.